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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/529,962	03/31/2005	Jurriaan Schmitz	BE02 0028 US	7450

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PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
1109 MCKAY DRIVE, M/S-41SJ
SAN JOSE, CA 95131

EXAMINER	
LEE, CHEUNG	
ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/529,962	SCHMITZ ET AL.	
	Examiner	Art Unit	
	Cheung Lee	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Notice to Applicant

1. Applicants' Amendment and Response to the Office Action mailed on May 26, 2006 has been entered and made of record.

2. In view of applicants' amendment to the drawing, the objection to the drawing has been withdrawn.

3. In view of applicants' amendment to the claim, the objection to claims 1-10 has been withdrawn.

4. In view of applicants' amendment to the claims, the rejection of claims 1-10 under 35 U.S.C. 112, second paragraph, has been withdrawn.

5. In view of applicants' amendments and arguments filed on May 26, 2006, the rejections of claims 1-10 under 35 U.S.C. 103(a) as stated in the indicated Office Action have been withdrawn. Applicants arguments have been rendered moot in view of the new or modified ground of rejection given below.

Claim Objections

6. Claim 11 objected to because of the following informalities:

In line 7, delete "the" before "silicon body".

In line 9, replace "the silicon oxide" with --a silicon oxide--.

In line 12, replace "dioxide" with --oxide--.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 3, 5, 9 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Ajuria et al. (US Pat. 5837612; hereinafter "Ajuria").

8. Referring to figures 6-12 and related text, Ajuria discloses [Re claim 1] a method of manufacturing a semiconductor device, the method comprising: applying an auxiliary layer 106 comprising non-doped silicon and germanium (col. 5, lines 55-60) to a surface of a silicon body 102 (see fig. 6) wherein, during an oxidation treatment (col. 6, lines 19-36), a thicker layer of silicon oxide 107b is formed on the auxiliary layer than is formed on the surface of the silicon body (see fig. 7); at the location of field isolation regions to be formed, forming windows in the in the auxiliary layer (see fig. 6) and grooves 108 in the surface of the silicon body; carrying out an oxidation treatment (col. 6, lines 19-36) to provide the walls of the grooves and of the windows respectively of the silicon body and the auxiliary layer with a layer of silicon oxide (see fig. 7), the silicon oxide 107b on the auxiliary layer being thicker than the silicon oxide 104 on the silicon body (col. 5, lines 45-55; col. 6, lines 29-37); but wherein it is precluded that the auxiliary layer adjacent to the windows is oxidized across the entire thickness (see fig. 7); after which, successively, a layer of isolating material 110a (col. 6, lines 37-45) is deposited in a thickness such that the grooves and the windows are filled completely (see fig. 8); and carrying out a planarization treatment (col. 6, line 53-col. 7, line 13) until the non-

oxidized part of the auxiliary layer is exposed (see fig. 10), after which this part of the auxiliary layer is removed (see fig. 11).

9. Referring to figures 6-12 and related text, Ajuria discloses [Re claim 11] a method of manufacturing a semiconductor device, the method comprising: applying an non-doped auxiliary layer 106 comprising silicon and germanium (col. 5, lines 55-60) to a substrate 102 including silicon (col. 5, lines 40-45), the non-doped auxiliary layer having oxidation characteristics that facilitate thicker oxide growth (col. 6, lines 19-36), relative to oxide growth on the substrate (see fig. 7); forming an opening 108 having walls extending through the auxiliary layer into silicon body (see fig. 6); oxidizing the auxiliary layer and the silicon body at the walls of the opening (col. 6, lines 19-36) to form a layer of silicon oxide 107b on the auxiliary layer that is thicker than a silicon oxide layer 104 on the silicon body, wherein the auxiliary layer adjacent to the wall is not oxidized across its entire thickness (see fig. 7); depositing a layer of isolation material 110a (col. 6, lines 37-45) on the layer of silicon oxide to fill the opening (see fig. 8); planarizing the semiconductor device (col. 6, line 53-col. 7, line 13) to expose a non-oxidized part of the auxiliary layer (see fig. 10); and after planarization, removing the non-oxidized part of the auxiliary layer (see fig. 11).

10. Ajuria discloses [Re claim 3] wherein the auxiliary layer is applied in a thickness (col. 5, lines 50-60) such that this layer is not converted across the entire thickness into an oxide during the oxidation treatment (see fig. 7).

11. Ajuria discloses [Re claims 5 and 9] wherein prior to applying the auxiliary layer to the surface of the silicon body, this surface is provided with a layer of silicon oxide 104, and the windows are also formed in the layer of silicon oxide (see fig. 6).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

12. Claims 2, 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ajuria, as applied above, and in view of Peterson et al. (US Pat. 6545299; hereinafter "Peterson").

13. [Re claim 2] Ajuria fails to disclose expressly wherein on the surface of the silicon body a layer of $Si_xGe_{1-x-y}C_y$, where $0.70<x<0.95$ and $y<0.05$, is provided as the auxiliary layer.

Peterso n discloses a material that comprises Si-Ge-C or Si-Ge (col. 3, lines 5-9), and Si-Ge-C refers to $Si_{1-x-y}Ge_xC_y$ (col. 2, lines 60-65). Peterson does not disclose expressly the value of x and y. However, any variation in stoichiometry of Si-Ge-C in the present claim is obvious in light of the cited art, because the changes in stoichiometry of Si-Ge-C produce no unexpected function. The routine varying of parameters to produce expected changes are within the ability of one of ordinary skill in the part. Patentability over the prior art will only occur if the parameter variation produces an unexpected result. *In re Aller, Lacey and Hall*, 105 USPQ 233, 235. *In re Reese* 129 USPQ 402, 406. Si-Ge is replaceable with Si-Ge-C, and Ajuria discloses germanium silicon layer (col. 5, lines 55-60). Therefore, it would have been obvious to use Si-Ge-C layer instead of germanium silicon layer since the two layers are equivalently used.

14. Ajuria discloses [Re claim 6] wherein the auxiliary layer is applied in a thickness (col. 5, lines 50-60) such that this layer is not converted across the entire thickness into an oxide during the oxidation treatment (see fig. 7).

15. Ajuria discloses [Re claim 8] wherein prior to applying the auxiliary layer to the surface of the silicon body, this surface is provided with a layer of silicon oxide 104, and the windows are also formed in the layer of silicon oxide (see fig. 6).

16. Claims 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ajuria, as applied above, and in view of Lam (US Pat. 6413828).

17. Ajuria discloses [Re claim 4] the window, which forms in the auxiliary layer (see fig. 6), but Ajuria fails to disclose expressly wherein a layer of silicon nitride is applied to the auxiliary layer, the windows being formed in the layer of silicon nitride.

Referring to figures 2A-2E and related text, Lam discloses a silicon nitride layer 108 on a middle polysilicon layer 106 (fig. 2A; col. 3, line 66-col. 4, line 11), and an opening in the silicon nitride (see fig. 2B).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a silicon nitride layer on an oxidizable layer, as taught by Lam, because it would have been to use nitride layer as a hard mask on the oxidizable layer controlling the oxidization area to fulfill the requirements of a specific application.

18. Ajuria discloses [Re claim 10] wherein prior to applying the auxiliary layer to the surface of the silicon body, this surface is provided with a layer of silicon oxide 104, and the windows are also formed in the layer of silicon oxide (see fig. 6).

19. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teaching Ajuria and Peterson, as applied above, and further in view of Lam.

Ajuria discloses [Re claim 7] the window, which forms in the auxiliary layer (see fig. 6), but Ajuria fails to disclose expressly wherein a layer of silicon nitride is applied to the auxiliary layer, the windows being formed in the layer of silicon nitride.

Referring to figures 2A-2E and related text, Lam discloses a silicon nitride layer 108 on a middle polysilicon layer 106 (fig. 2A; col. 3, line 66-col. 4, line 11), and an opening in the silicon nitride (see fig. 2B). The motivation stated in claim 4 also applies.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cheung Lee whose telephone number is 571-272-5977. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cheung Lee

August 3, 2006

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER